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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,689	12/03/2001	Hiroaki Asuma	501.40910X00	6641

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EXAMINER

NGUYEN, CHANH DUY

ART UNIT PAPER NUMBER

2675

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/998,689

Applicant(s)

ASUMA ET AL.

Examiner

Chanh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4 and 5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4 and 5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/29/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed on October 29, 2005 has been entered and considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al (U.S. Patent No. 5,907,314) in view of Seo (U.S. Patent No. 5,742,365).

As to claim 1, Negishi discloses a display device as recited in claim 1 with exception of describing the limitation "the gate signal line is a light shielding member

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". For example, Negishi teaches gate signal lines (X1-Xn) which are extended in the x direction and are arranged in parallel in the y direction, scanning signal driving circuits (115, 116) which supply scanning signals to respective gate signal lines (X1-Xn). Negishi clearly teaches the arrangement of gate lines and scan driving circuits in Figure 11 is same as applicant's disclosed device in Figures 1 and 11. Negishi teaches drain signal lines (Y1-Yn) which are extended in the y direction and are arranged in parallel in the x direction, and video signal driving circuits (112-113) which supply video signals to respective drain signal lines (Y1-Yn) are formed on one surface of an insulating substrate (e.g., glass substrate 103).

Negishi teaches the display device (101) including a thin film transistor (105a) which is driven by the scanning signals from one side of the gate signal line and a pixel electrode to which the video signals from one side drain of the signal line are supplied through this thin film transistor in each pixel region which is surrounded by the respective signal lines. Negishi teaches the display region (102) which is a collection of the pixel regions is divided into two separate display regions (upper half of liquid crystal panel 102 and lower half of liquid crystal panel 102) using an imaginary line extending along the x direction as a boundary (see Figure 11).

Negishi teaches the scanning signal driving circuit (115) which supplies the scanning signals to respective gate signal lines in one display region (e.g., upper half of the liquid crystal) and the scanning signal driving circuit (116) which supplies the scanning signals to respective gate signal lines in the other display region (e.g., lower half of the liquid crystal) being separately formed. Negishi teaches the drain signal

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lines at one display region side are separated from the drain signal lines at the other display region (see Figure 11). Negishi teaches the video signal driving circuit (115-116) which supplies the video signals to respective drain signal lines in one display region and the video signal driving circuit which supplies the video signals to respective drain signal lines in the other display region are separately formed (see Figure 11).

Negishi teaches the area (i.e. area between X_m and X_{m+1}) which divides respective drain signal lines (Y_1 - Y_n) of one display region (e.g., upper half of display panel 102) and respective drain signal lines (Y_{11} - Y_{nn}) of the other display regions side (e.g., lower half of display panel 102) being position over the gate signal line (i.e. X_m or X_{m+1}). Negishi clearly teaches the area (i.e. area between X_m and X_{m+1}) separated end portions of respective drain signal lines at one display region side (e.g., end portion of signal line Y_1 intersect with gate X_m at upper display panel 102) and separated end portions of respective drain signal lines at other display region (e.g., end portion of signal line Y_{11} intersect with gate X_{m+1}) all superposed on the gate lines (i.e. end portion of signal line Y_1 intersects with gate X_m , and end portion of signal line Y_{11} intersect with gate X_{m+1}). The claimed "superposed on the gate lines" is broad enough to read on Y_1 intersecting with X_m and Y_{11} intersecting with X_{m+1} . The claim does not require superposed on a single gate line".

The only different the reference of Negishi and the claimed invention is that Negishi does not mention insulation film and light shielding member. Seo teaches an intervening insulation film (3) being formed between the gate lines (2) and the drain

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signal line (6). Seo also teaches the gate signal line (2) being a light shielding member by using black resin (19) deposited around the gate electrode (2) (see column 5, lines 49-54 and column 6, lines 35-38). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used the light shielding member gate signal line to the gate signal line of Negishi because the black resin not only shields light, but also serves as the gate insulation film for insulating the gate. Thus, the thickness of the gate insulating film can be reduced (see column 6, lines 35-38 of Seo).

As to claim 2, it is clear that Negishi teaches the display device being provided with power supply changeover means which drives the scanning signal driving circuit and the video signal driving circuit at one display region side and the scanning signal driving circuit and the video signal driving circuit at the other display region side together or drives the scanning signal driving circuit and the video signal driving circuit at only one of both display regions as recited in the claim.

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi in view of Seo, as applied to claim 1, and further in view of Yamazaki (U.S. Patent No. 6,490,562).

6. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi in view of Yasuda as applied to claim 1 above, and further in view of Yamazaki.

As to claims 4-5, note the discussion of Negishi and Seo above. Both do not mention the limitation the scanning signal lines being supplied to the gate lines sequentially in the direction moving away from respective gate signal at the boundary of one display region and the other display region. Yamazaki teaches the scanning signal lines are supplied to the gate lines sequentially in the direction moving away from respective gate signal at the boundary of one display region and the other display region (see figure 9A). Yamazaki clearly teaches the video signals being supplied from the video signal driving circuit in synchronism with the supply of the scanning (see 2, lines 7-15). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used scanning moving away from boundary of on display region and the other display region as taught by Yamazaki to the scanning circuit of Negishi as modified by Seo so that a high speed, large area display with high information content can be easily accomplished at low cost (see column 3, lines 40-49 of Yamazaki).

Response to Arguments

7. Applicant's arguments with respect to claims 1-2 and 4-5 have been considered but are moot in view of the new ground(s) of rejection.

In view amendment, the reference of Seo has been added for new ground of rejection.

Applicant argues that Nigishi does not teach the limitation the area which divides respective drain signal lines of one display region side and respective drain signal lines of the other display region side is positioned over the gate signal line and separated end

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portions of respective drain signal lines at one display region side and separated end portions of respective drain signal lines at the other display region side are all superposed on the gate signal lines. However, the claimed "superposed on the gate lines" is broad enough to read on Y1 intersecting with X_m and Y11 intersecting with X_{m+1} as set forth in the rejection. The claim does not require superposed on a single gate line".

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

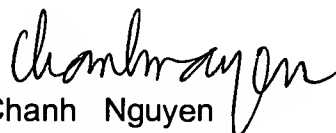
Inquiries


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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (571) 272-7772. The examiner can normally be reached on Monday- Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Chanh Nguyen
Primary Examiner
Art Unit 2675


C. Nguyen
April 15, 2005